ABSTRACT

FAST ANALOGUE-TO-DIGITAL CONVERTER

The invention relates to the fast analogue-to-digital converters having differential inputs and a parallel structure, comprising at least one network of N series resistors with value r and one network of N comparators.

In order to minimize the influence of parasitic capacitances of the resistor network on the comparator response time, it is provided that the series resistor network receives a reference voltage (VH) and is traversed by a fixed current I_0 and that the row i (i varying from 1 to N) comparator ($COMP_i$) essentially comprises a dual differential amplifier with four inputs; two inputs receive a differential voltage VS-VN to be converted, a third being connected to a row i resistor of the network, and a fourth input being connected to an N-i row resistor of the network. The dual differential amplifier supplies a voltage representing a difference of the form (VS-VSN) − (N-2i)r.I_0, and the comparator switches in one direction or the other depending on the level of the voltage VS-VSN and on the row i of the comparator when said difference changes sign.

Figure 2